ITS 323 – QUIZ 4(2)

First name: _____   Last name: _____

ID: _____   Total Marks: _____

<div align="right">out of 10</div>

Question 1 [4 marks]

   a) Queuing delay may occur in packet switches if multiple input lines are sending to the same output line at the same time.

                                                                            True   False

   b) A virtual circuit packet switch may reserve resources for a connection during connection setup.

                                                                            True   False

   c) In routing, increasing the amount of information about the network that is available to nodes, will increase the overheads introduced into the network by routing protocols.
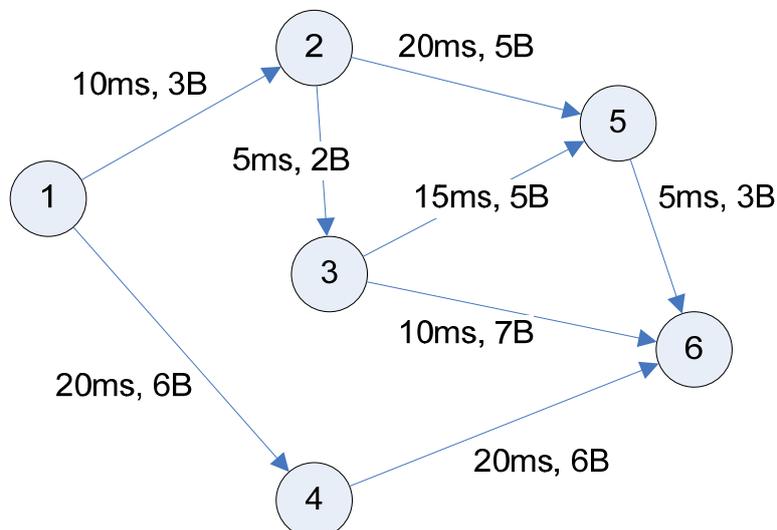
                                                                            True   False

   d) With datagram packet switching, increasing the packet size will result in shorter delays because of the reduced overhead of headers

                                                                            True   False

**Question 2** [2 marks]

Consider the network below.

The delay (in milliseconds) and price (in Baht per MB) of each simplex link is shown. If a routing algorithm chose a path from 1 to 6 to be 1 – 2 – 3 – 6 then what metric was used by the least cost routing algorithm (select no more than one answer):

   i.   Hops

   ii. Delay

   iii. Price

Question 3 [4 marks]

Compare the delay in sending data using Circuit Switching versus Datagram Packet Switching as shown below.
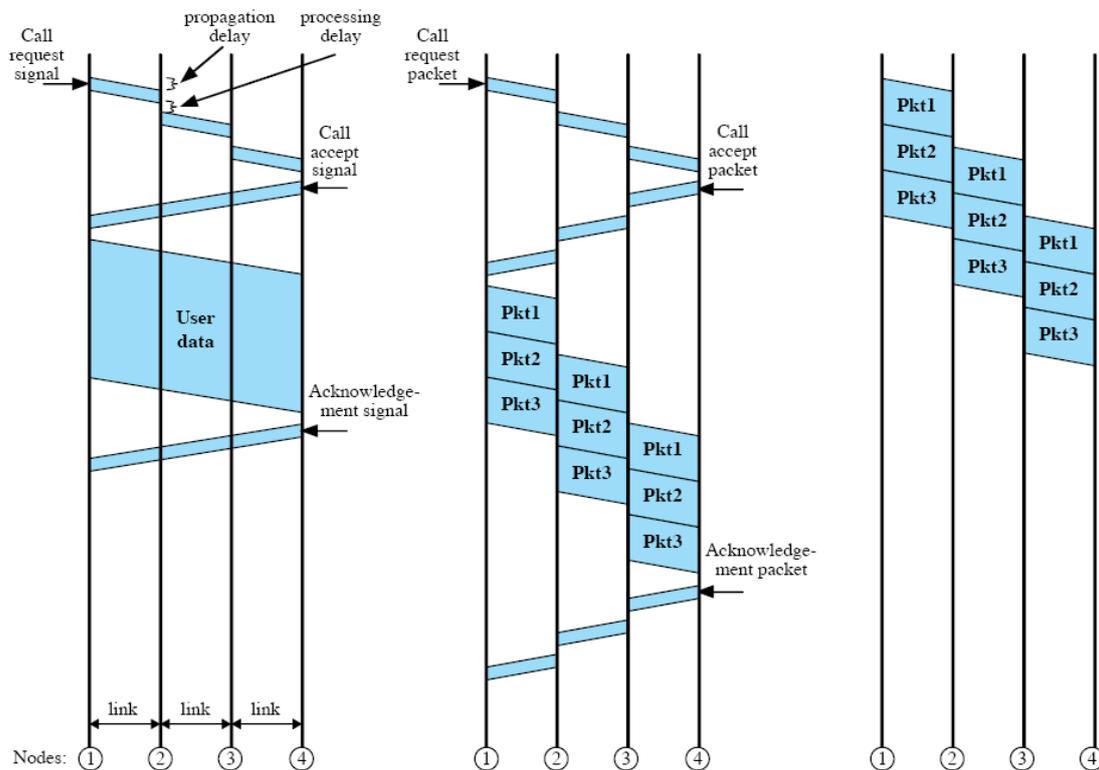
You may assume:

- Number of links, **L** = 5
- Packet Switching:
  - Entire packet consists of Header and Data
  - Header transmission time, **H** = 1ms
  - Data transmission time, **D** = 15ms
  - Number of packets is **P** = 10
- Circuit Switching:
  - Time between sending call request signal until receiving call accept signal is **C** = 20ms.
  - Time between sending and receiving the call acknowledgment is **A** = 10ms.
- All other processing, propagation and queuing delays are 0.

a) What is the total delay for Datagram Packet Switching? [2 marks]

b) What is the total delay for Circuit Switching (assuming same amount of data to be sent as in Datagram Packet Switching above)? [2 marks]